CLAIMS

What is claimed is:

1. A router including buffers, for information units transferred through the router, comprising:

a first set of rapidly accessible buffers for the information units; and

a second set of buffers for the information units that are accessed more slowly than the first set.

2. A router as claimed in claim 1 wherein:

the router is implemented on one or more integrated circuit chips;

the first set of buffers is located on the router integrated circuit chips; and

the second set of buffers is located on memory chips separate from the router integrated circuit chips.

3. A router as claimed in claim 1 where the second set of buffers holds information units for a complete set of virtual channels.

4. A router as claimed in claim 1 wherein the first set of buffers comprises:

a buffer pool; and

a pointer array.

5. A router as claimed in claim 1 wherein the first set of buffers is organized as a set-associative cache.

6. A router as claimed in claim 5 wherein each entry in the set associative cache contains a single information unit.

7. A router as claimed in claim 5 wherein each entry in the set associative cache contains the buffers and state for an entire virtual channel.

8. A router as claimed in claim 1 further comprising flow control to stop the arrival of new information units while transferring information units between the first set of buffers and the second set of buffers.

9. A router as claimed in claim 8 wherein the flow control is blocking.

10. A router as claimed in claim 8 wherein the flow control is credit-based.

11. A router as claimed in claim 1 further comprising miss status registers to hold information units waiting for access to the second set of buffers.

12. A router as claimed in claim 1 further comprising an eviction buffer to hold entries staged for transfer from the first set of buffers to the second set of buffers.

13. A router as claimed in claim 1 in a multicomputer interconnection network.

14. A router as claimed in claim 1 in a network switch or router.

15. A router as claimed in claim 1 wherein the router is a fabric router and the information units are flits.

16. A method of buffering information units in a router comprising:

storing the information units in a first set of rapidly accessible buffers; and

storing overflow from the first set of buffers in a second set of buffers that are accessed more slowly than the first set.

17. A method as claimed in claim 16 wherein

the router is implemented on one or more integrated circuit chips;

the first set of buffers are located on the router integrated circuit chips; and

the second set of buffers are located on memory chips separate from the router integrated circuit chips.

18. A method as claimed in claim 16 where the second set of buffers holds information units for a complete set of virtual channels.

19. A method as claimed in claim 16 further comprising, in the first set of buffers, storing the information units in a buffer pool shared by channels and pointing to information units within the buffer pool from an array of pointers associated with individual channels.

20. A method as claimed in claim 16 wherein the first set of buffers is organized as a set-associative cache.

21. A method as claimed in claim 20 wherein each entry in the set associative cache contains a single information unit.

22. A method as claimed in claim 20 wherein each entry in the set associative cache contains the information unit buffers and state for an entire virtual channel.

23. A method as claimed in claim 16 further comprising controlling flow to stop the arrival of new information units while transferring flits between the first set of buffers and the second set of buffers.

24. A method as claimed in claim 23 wherein the flow control is blocking.

25. A method as claimed in claim 23 wherein the flow control is credit-based.

26. A method as claimed in claim 16 further comprising storing information units waiting for access to the second set of flit buffers in miss status registers.

27. A method as claimed in claim 16 further comprising storing information units staged for transfer from the first set of buffers to the second set of buffers in an eviction buffer.

28. A method as claimed in claim 16 wherein the router is in a multicomputer interconnection network.

29. A method as claimed in claim 16 wherein the fabric router is in a network switch or router.

30. A method as claimed in claim 16 wherein the router is a fabric router and the information units are flits.

31. A network comprising a plurality of interconnected routers, each router including information unit buffers comprising:

a first set of rapidly accessible information unit buffers; and

a second set of information unit buffers that are accessed more slowly than the first set.

32. A network as claimed in claim 31 wherein:

the router is implemented on one or more integrated circuit chips;

the first set of buffers are located on the router integrated circuit chips; and

the second set of buffers are located on memory chips separate from the router integrated circuit chips.

33. A network as claimed in claim 31 where the second set of buffers holds information units for a complete set of virtual channels.

34. A network as claimed in claim 31 wherein the first set of buffers comprises:

a buffer pool; and

a pointer array.

35. A network as claimed in claim 31 wherein the first set of buffers is organized as a set-associative cache.

36. A network as claimed in claim 31 further comprising flow control to stop the arrival of new information units while transferring information units between the first set of buffers and the second set of buffers.

37. A network as claimed in claim 31 further comprising flow control to stop the arrival of new information units while transferring flits between the first set of buffers and the second set of buffers.

38. A network as claimed in claim 31 in a network switch or router.

39. A network as claimed in claim 31 wherein the router is a fabric router and the information units are flits.

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40. A router comprising:

means for storing information units in a first set of rapidly accessible buffers; and

means for storing information units in a second set of buffers that are accessed more slowly than the first set.

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41. A router as claimed in claim 40 where the second set of buffers holds information units for a complete set of virtual channels.

42. A router as claimed in claim 40 wherein the first set of buffers comprises:

a buffer pool shared by channels; and

means for pointing to entries in the buffer pool for individual channels.

43. A router as claimed in claim 40 wherein the first set of buffers is organized as a set-associative cache.

44. A router as claimed in claim 40 further comprising means for providing flow control for stopping the arrival of new information units while transferring information units between the first set of buffers and the second set of buffers.

45. A router as claimed in claim 40 wherein the router is a fabric router and the information units are flits.

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